REMARKS

I. Introduction

Applicant notes that the reference carrying the designated ID:AZ, which was submitted in the Information Disclosure Statement "IDS" filed on November 25, 2003, has not yet been indicated to have been considered by the Examiner. Applicant also notes that the Examiner has not been provided a copy of this reference. Although Applicant believes that a copy of the foregoing reference has been furnished at the time when the IDS was filed, an additional copy is enclosed herewith for the Examiner's convenience. It is respectfully requested that the Examiner initial this reference on the PTO-1449 form and return the form to the Applicant so as to confirm that the reference has been considered.

For the reasons set forth below, Applicant respectfully submits that all pending claims are patentable over the cited prior art references.

II. The Rejection Of Claims 13, 21 and 22 Under 35 U.S.C. § 103

Claims 13, 21 and 22 are rejected as allegedly unpatentable over JP 411205043A to Irie in view of USP No. 5,973,539 to Komurasaki, and further in view of USP No. 5,678,226 to Li and USP No. 6,466,775 to Franca-Neto. Applicant respectfully traverses this rejection for at least the following reasons.

A. Li Does Not Disclose Drains Of First And Second Transistors Are Coupled To The Common Node

Claim 13 recites in-part a common node for at least one of the first radio frequency input signal and the second radio frequency input signal and an intermediate frequency output signal, wherein ***drains of the first and second transistors are coupled to the common node.***

In the pending rejection, the Examiner admits that the combination of Irie and Komurasaki does not disclose a common node having the foregoing claimed features, and relies on Li to cure these deficiencies. Applicant respectfully disagrees.

It is noted that the pending rejection broadly reads the node to the left of the capacitor C4 of Li as the claimed common node, and asserts that the drain of transistor 12 and the intermediate frequency signal port 20 are coupled to this node. However, the pending rejection appears to inadvertently ignore the fact that claim 13 requires the drains of ***two*** separate and distinct transistors (namely, the first and the second transistors) to be coupled to a common node. Accordingly, at best, the rejection has only demonstrated that a ***single*** transistor is coupled to the alleged node, but failed to illustrate ***two*** transistors being coupled to this node (see, Fig. 2). Franca-Neto does not cure this defect of Li, because this reference does not teach or suggest a common node that connects a radio frequency input signal and an intermediate frequency output signal.

For at least these reasons, it is respectfully submitted that the combination of Irie, Komurasaki, Li and Franca-Neto, alone or in combination, do not disclose a common node having drains of a first transistor and a second transistor coupled thereto, as recited in claim 13.

B. Franca-Neto Does Not Disclose An Interconnection Circuitry

Claim 13 further recites in-part an interconnection circuitry to turn off a second transistor when a ***first local oscillator input signal*** is applied to a first transistor and to turn off the first transistor when a ***second local oscillator input signal*** is applied to a second transistor.

In the pending rejection, the Examiner asserts that Franca-Neto discloses the foregoing claimed features at col. 5, lines 35-39. Applicant, again, respectfully disagrees. Specifically, it is respectfully submitted that the mixer disclosed at Fig. 1D, as discussed in the alleged section of Franca-Neto, and the claimed interconnection circuitry are functionally and structurally different.

As noted in the neighboring paragraphs of the cited section, Franca-Neto discloses a core of a mixer having transistors 155-157. Specifically, the gate of transistor 155 receives a negative phase of ***a local oscillator signal*** and a negative phase of a RF signal (see, col. 5, lines 25-27). Similarly, the gate of the transistor 156 receives a positive phase of ***the local oscillator signal*** and a negative phase of the RF signal (see, col. 5, lines 27-29), such that the local oscillator

signal alternatively turns "ON" and "OFF" transistors 155 and 156. That is, the local oscillator signal input to the transistors 155 and 156 is the ***same*** signal. Franca-Neto expressly uses the positive phase and the negative phase of the ***same*** oscillator signal to drive the transition states of the transistors 155 and 156.

Accordingly, the core mixer of Franca-Neto, as shown in Fig. 1D, is functionally and structurally different from the claimed interconnection circuitry, because the claimed interconnection circuitry turns off two transistors using ***two*** separate and distinct oscillator input signals, whereas the core mixer of Franca-Neto turns on and off transistors 155 and 156 using a ***single*** oscillator signal with different phases.

Absent these teachings, it is respectfully submitted that the combination of Irie, Komurasaki, Li and Franca-Neto, alone or in combination, do not disclose an interconnection circuitry to turn off a second transistor when a first local oscillator input signal is applied to a first transistor and to turn off the first transistor when a second local oscillator input signal is applied to a second transistor, as recited in claim 13.

As noted in **M.P.E.P. § 2143.03** under the section entitled "All Claim Limitations Must Be Taught or Suggested," which sets forth the applicable standard:

> To establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. (citing *In re Royka*, 180 USPQ 580 (CCPA 1974)).

In the instant case, the pending rejection does not "establish prima facie obviousness of [the] claimed invention" as recited in claim 13 because the proposed combination fails the "all the claim limitations" standard required under the meaning of 35 U.S.C. § 103.

C. Irie and Komurasaki Do Not Provide The Requisite Motivation

Applicant would initially stress the requisite motivation to support the ultimate legal conclusion of obviousness under 35 U.S.C. §103 is not an abstract concept but must stem from the applied prior art as a whole and have realistically impelled one having ordinary skill in the art to modify a reference or combine references to arrive at a claimed invention. *In re Newell*, 891 F.2d 899, 13 USPQ2d 1248 (Fed. Cir. 1989). It has been judicially held that a ***generalization***

does ***not*** establish the requisite motivation to modify a specific reference in a specific manner to arrive at a specifically claimed invention. *In re Deuel*, 51 F.3d 1552, 34 USPQ2d 1210 (Fed. Cir. 1995). Rather, the PTO is required to point out wherein the prior art suggests modifying a reference or combining references to arrive at a specifically claimed invention. *In re Rouffet*, 149 F.3d 1350, 47 USPQ2d 1543 (Fed. Cir. 1998). In this respect, Applicant would further stress that the ***mere identification*** of claim features in disparate references does not establish the requisite realistic motivation to support the ultimate legal conclusion of obviousness under 35 U.S.C. §103. *Grain Processing Corp. v. American-Maize Products Co.*, 840 F.2d 902, 5 USPQ2d 1788 (Fed. Cir. 1988).

The PTO has offered ***no*** explanation ***why*** one having ordinary skill in the art would somehow have been lured to go against the express objectives given by Irie to modify the node thereof in the manner recited by the pending claims. *In re Rouffet*, supra.; *In re Mayne*, supra. Thus, it is clear that the PTO has not established a *prima facie* basis to deny patentability to the claimed invention under 35 U.S.C. §103.

In the instant case, the purported motivation to modify Irie using Komurasaki (i.e., "...so that the power supply voltage can be reduced") offered by the Examiner is defective. The Office Action attempts to overcome the deficiency in Irie by asserting an opinion that one of ordinary skill in the art would have found it obvious to improve the power supply of Irie.

However, there is no suggestion or support in the prior art that the mixer circuit of Irie requires a reduction in power supply. As is apparent, Irie has provided ***no*** discussion regarding power supply voltage, let alone a method for reducing such voltage. As such, Applicant respectfully submits that the PTO has failed to discharge initial burden of identifying any basis of record upon which to predicate the conclusion that one having ordinary skill in the art would have been realistically impelled to modify the mixer circuit of Irie to arrive at the claimed invention, let alone doing so by using two transistors to mix two local oscillator input signals with two radio frequency input signals. *In re Mayne*, 104 F.3d 1339, 41 USPQ2d 1451 (Fed. Cir. 1997). Thus, a *prima facie* case of obviousness has not been established using Irie.

In this regard, the pending rejection has inadvertently overlooked the fact that the alleged motivation is ***only applicable*** to circuits that employ "vertically connected two stages of differential transistor pairs (see, col. 3, lines 10-12). As is evident from Irie that ***no*** such differential transistors are employed, it is inevitable that the alleged motivation is improper.

Thus, there is no disclosed need, desire or purpose for reducing the power supply voltage of Irie any more than what has already been disclosed. Accordingly, the alleged motivation for making the proposed modification is factually nonexistent.

D. Irie, Komurasaki and Li Do Not Provide The Requisite Motivation

Furthermore, the purported motivation (i.e., "...so that circuit design can be simplified") offered by the Examiner using the Li reference is defective. The Office Action attempts to overcome the deficiency in Irie by asserting an opinion that one of ordinary skill in the art would have found it obvious to simplify the mixer circuit of Irie.

However, there is no suggestion or support in the prior art that the common node would act to simplifier the mixer circuit of Irie. It is respectfully submitted that modifying the mixer circuit of Irie by adding the alleged common node as disclosed in Li would actually make the mixer circuit of Irie more complex than simpler, as new electrical connections would be introduced. In addition, it should be noted that the alleged motivation is not even required in the method of mixer because the mixer circuit of Irie disclosed therein already has the means by which to simplify the circuit design (e.g., in paragraph [0022] in which Irie discloses that without being accompanied by an increase of a circuit scale, a mixer circuit is derived where control of interference by image frequency can be implemented).

Thus, there is no disclosed need, desire or purpose for making the mixer circuit of Irie any more simplistic than already disclosed by Irie. Accordingly, the alleged motivation for making the proposed modification is factually nonexistent.

E. Modification of Irie, Komurasaki and Li Using Franca-Neto

With respect to Franca-Neto, it is respectfully submitted that the proposed combination relies on modifying ***a modifying reference***, which is submitted to be too attenuated from the claimed invention to be considered obvious. Specifically, the Examiner first modifies Irie with Komurasaki to add a first transistor to mix a first local oscillator with the radio frequency signal of Irie and a second transistor to mix a second local oscillator with the radio frequency signal of Irie. Next, the Examiner proceeds to modify Komurasaki to add a common node such that the alleged first and second transistors are coupled thereto. Then, the combination of Irie, Komurasaki and Li is modified using Franca-Neto. Then, Franca-Neto is introduced to modify Komurasaki to add an interconnection circuitry so that the alleged first and second transistors can be turned on and off based on oscillator signals.

Although it is understood that there is no limit to the number of references that can be used in combination for rejecting a claim, it is submitted that a secondary reference cannot be used to reject the feature of another ***secondary*** reference. In the instant case, the Examiner modifies the transistors of Komurasaki with the teachings of another secondary references and Li Franca-Neto, rendering the proposed modifications non-obvious as being too far removed from the claimed invention (i.e., Examiner's need to modify a secondary reference to reach the claimed invention is itself an indicia of non-obviousness of the modification).

Lastly, similar to the reasoning set forth above with respect to Komurasaki, the alleged motivation (i.e., "... to provide a highly linear and low voltage mixer") as asserted by the Examiner is completely ***irrelevant*** and ***unrelated*** to the mixer circuit rendered by the modification of Irie using Komurasaki and Li. Indeed, Franca-Neto expressly discloses that highly linear operation of a mix is obtained by selecting three different transistors among seven transistors such that the transconductance of one of the selected transistors is substantially equal to the sum of the transconductance of the other two selected transistors (see, e.g., col. 4, lines 62-66). As is apparent, neither Irie, Komurasaki nor Li disclose or suggest a mixer circuit suing seven transistors. Accordingly, Irie, Komurasaki nor Li do not disclose any need for a linear,

low voltage mixer as desired by Franca-Neto. Thus, Applicant respectfully submits that a *prima facie* case of obviousness has not been established using Franca-Neto.

III. All Dependent Claims Are Allowable Because The Independent Claims From Which They Depend Are Allowable

Under Federal Circuit guidelines, a dependent claim is neither anticipated nor rendered obvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, *Hartness International Inc. v. Simplimatic Engineering Co., 819 F.2d at 1100, 1108 (Fed. Cir. 1987).* Accordingly, as independent claims 13, 21 and 22 are patentable for the reasons set forth above, it is respectfully submitted that all claims dependent thereon are also in condition for allowance.

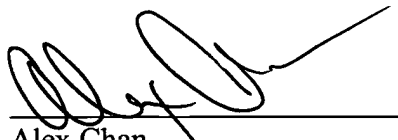
IV. Conclusion

Accordingly, it is urged that the application is in condition for allowance, an indication of which is respectfully solicited.

If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicant's attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 06-1050 and please credit any excess fees to such deposit account.

Respectfully submitted,



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A HIGHLY INTEGRATED MONOLITHIC X-KU BAND UPCONVERTER

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ABSTRACT

This paper describes a monolithic upconverter with a high level of integration (87 components), operating in the X-Ku band. It consists of a two-stage RF amplifier; a broadband, transformer-coupled, double-balanced Schottky diode mixer; and a two-stage LO buffer amplifier. The chip measures only 96x48 mils.

The upconverter IC, packaged along with MMIC amplifiers has been tested at different LO frequencies between 8-15 GHz with a swept IF from 200 MHz to 1.5 GHz, and typically has 10 dB of conversion gain for upconverted output across the 8-16.5 GHz band.

INTRODUCTION

Microwave frequency converters are widely used in commercial and military communication systems. Until now, the MMIC frequency converter effort has been focused on the downconversion of frequencies (1, 2, 3,) with some effort on upconversion (4, 5). Upconverters are also an essential part of microwave communication and EW systems.

This paper discusses the first fully monolithic frequency upconverter in the X-Ku band with a high level of integration : 26 spiral inductors, 25 resistors, 24 MIM capacitors, 8 FETs and 4 diodes. The unique features of this design are lumped-element matching with accurate modeling at X-Ku band and a push-pull design approach. This monolithic converter is designed for a 15 GHz transmitter for a digital radio communication system application.

In terms of cost, size, weight, and reliability, this monolithic upconverter is superior to its MIC counterpart.

THEORY OF OPERATION OF AN UPCONVERTER

For frequency upconversion, the low-frequency input signal is fed into the IF (intermediate frequency) port of the mixer. After mixing with the high frequency local oscillator (LO) signal, the upconverted high-frequency signal comes out of the RF port.

The I-V characteristics of a Schottky barrier diode in a mixer are given by:

$$I = I_0 (e^{qv/kt} - 1) \quad (1)$$

Using series expansion for $e^{qv/kt}$ as:

$$e^{qv/kt} = 1 + qv/kt + (qv/kt)^2/2! + (qv/kt)^3/3! + \ldots \quad (2)$$

we can rewrite Equation (1) as:

$$I = a_0 + a_1 v + a_2 v^2 + \ldots + a_n v^n \quad (3)$$

where ao, a_1, a_2...are constants and v is the applied voltage across the diode. Let the LO input voltage waveform be $v_1 \sin w_1 t$ and the low-frequency input voltage waveform to the IF port be represented by $v_2 \sin w_2 t$.

Additive mixing of the input low-frequency signal and the LO signal gives the voltage waveform of the diode as:

$$v = v_1 \sin w_1 t + v_2 \sin w_2 t \quad (4)$$

Inserting the value of v from Equation (4) into Equation (3), we get:

$$I = a_0 + a_1 (v_1 \sin w_1 t + v_2 \sin w_2 t) + a_2 (v_1 \sin w_1 t + v_2 \sin w_2 t)^2 + a_3 (v_1 \sin w_1 t + v_2 \sin w_2 t)^3 + \ldots \quad (5)$$

The square term in the above equation can be expanded as:

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$$a_2 (v_1 \sin w_1 t + v_2 \sin w_2 t)^2 = a_2 v_1^2 \sin^2 w_1 t + a_2 v_2 \sin^2 w_2 t + a_2 v_1 v_2 [\cos (w_1 - w_2)t - \cos (w_1 + w_2)t] \quad (6)$$

From Equation (6), we see that both the sidebands, [upper $(w_1 + w_2)$ and lower $(w_1 - w_2)$], are present along with other higher order products. Suitable filtering can be used at the output to suppress the unwanted sideband as well as the LO.

UPCONVERTER CHIP DESCRIPTION

This monolithic upconverter chip is comprised of a two-stage, 8-16 GHz RF amplifier; a two-stage, 8-16 GHz LO buffer amplifier; and a transformer-coupled wideband, double-balanced Schottky diode mixer. There is no amplifier at the IF input port as shown in the block diagram in Figure 1.

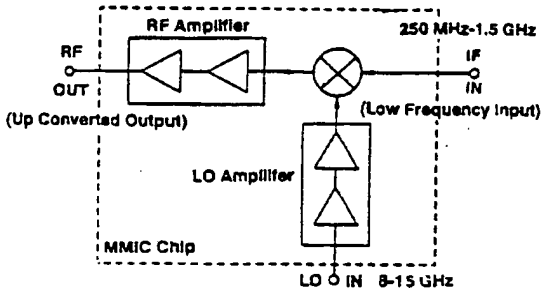

Figure 1 Block Diagram of the Monolithic X-Ku Band Upconverter

Since the diode mixers do not have a good wideband match, the LO amplifier is needed to provide a good match at the LO port. This helps to reduce conversion gain variations due to mismatches, and also reduces the LO input power requirement. Similarly, the RF amplifier at the output amplifies the upconverted signal and provides a good output match and higher output power. These high-frequency amplifiers are best integrated on the same chip since long bond wires between chips can cause large gain and phase variations from unit to unit at high frequencies.

The two-stage, push-pull RF amplifier is designed for operation in the 8-16 GHz band. The push-pull design-- with an inherent virtual ground in the middle-- allows low-inductance grounds to be realized without the use of via-holes. The absence of via-holes simplifies the process and augments MMIC chip yields. The push-pull amplifier is also well-suited for driving a double-balanced mixer.

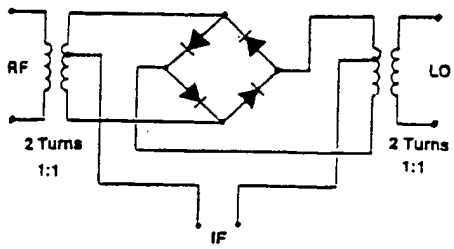

Figure 2 Schematic of a Double-Balanced Schottky Diode Mixer

We have used the lossy match technique to obtain flat gain response and good match over the octave bandwidth. The RF amplifier characterized separately provides 8 $\pm$ 1 dB gain over the 8-16 GHz band, while drawing 40 mA from an 8 V supply. The input and output VSWRs are less than 2:1.

The LO buffer amplifier is a similar 8-16 GHz, 2-stage, push-pull amplifier. It also uses an 8 V supply and draws 50 mA. It has been designed to deliver the required drive power (about 10 dBm) to the mixer. The mixer used is a transformer-coupled, double-balanced Schottky diode mixer (Figure 2).

Planar transformers are used to couple signals into the diode quad consisting of 1-micron gate-interdigitated, GaAs Schottky diodes. The mixer response measured separately showed 8-10 dB of conversion loss over the 8-16 GHz band. A photograph of the upconverter IC is shown in Figure 3.

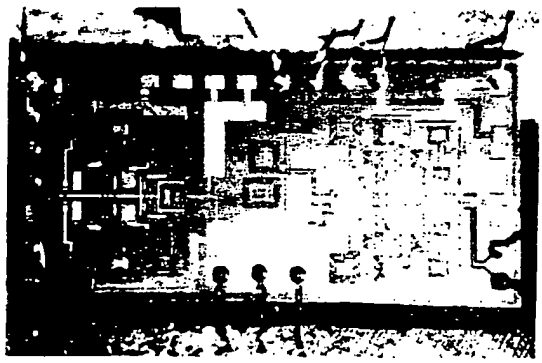

Figure 3 Photograph of the Monolithic Upconverter Chip

RESULTS

This upconverter chip has been characterized both at the wafer level and in a package. Wafer level test data exhibit excellent RF yield (>70%).

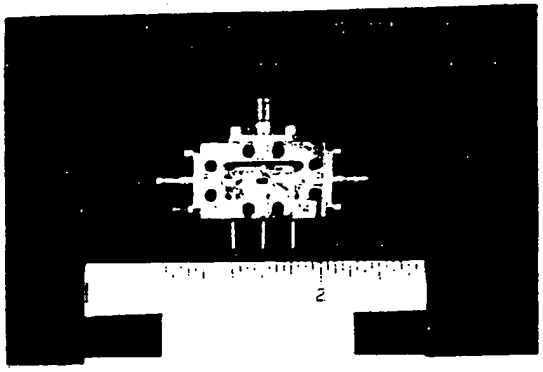

Figure 4 Photograph of the Packaged Upconverter IC

The upconverter IC, along with its necessary MIC baluns and additional amplifiers at the RF and IF ports, has been assembled in an SMA Package. Figure 4 is a photograph of the packaged upconverter IC.

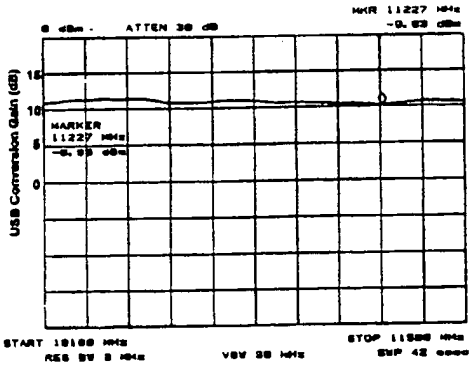

Figure 5 The Output Spectrum of the Packaged Upconverter with a 10 GHz LO

Figure 5 shows the measured results for the USB on the upconverter module with the LO centered at 10 GHz, and the input frequency swept from 200 MHz to 1.5 GHz. The module has 11 dB of conversion gain. The gain flatness is within $\pm$ 1 dB. Both the LSB and USB are available. The desired sideband can be chosen using the proper filter.

With a 15 GHz LO and the same swept input frequency, the module shows 10 dB of conversion gain (Figure 6). With an 8 GHz LO, the conversion gain is approximately 9 dB.

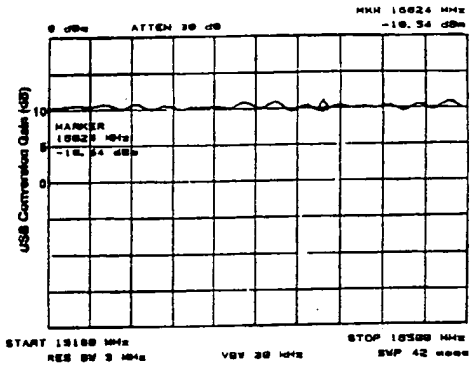

Figure 6 The Output Spectrum of the Packaged Upconverter with a 15 GHz LO

For a constant IF input frequency of 500 MHz, the upconversion gain is 10 $\pm$1 dB over the 8-15 GHz band (Figure 7). The two-tone intermodulation products measured with two equal amplitude input signals (-20 dBm) separated by 5 MHz and a 14 GHz LO are shown in Figure 8. The third-order intermodulation product level is -46 dBc, and the third-order intercept point at the output is 13 dBm.

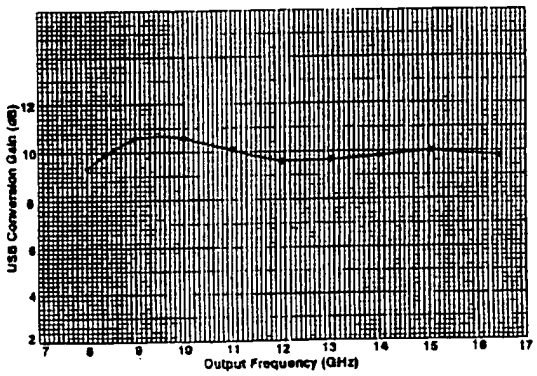

Figure 7 The USB Conversion Gain of the Upconverter Module over the 8-16 GHz band.

The output power at 1 dB gain compression has been measured to be 4.5 dBm at the high end of the band. The maximum VSWR measured at the module level for the low-frequency (0.1 - 1.5 GHz) input port is 2.5:1, the upconverter port is 2.0:1, and the LO port is 2.0:1, respectively.

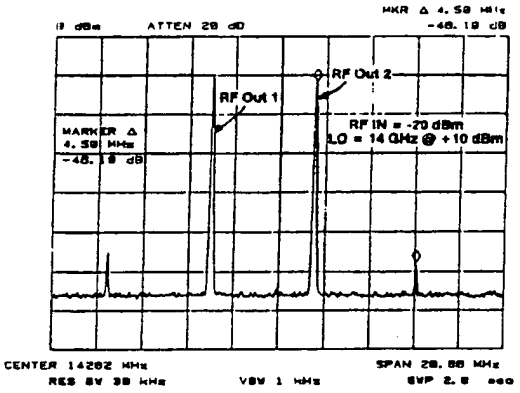

Figure 8 The Two-Tone Third Order Intermodulation Products with a 14 GHz LO

CONCLUSIONS

A fully monolithic upconverter with a high level of integration has been developed for 8-16 GHz operation. This monolithic upconverter demonstrated high yield and is suitable for low-cost, high-volume system applications.

ACKNOWLEDGEMENT

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